DØ RunIIb Upgrade Status

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for the DØ RunIIb Upgrade Project

PAC
December 13, 2003

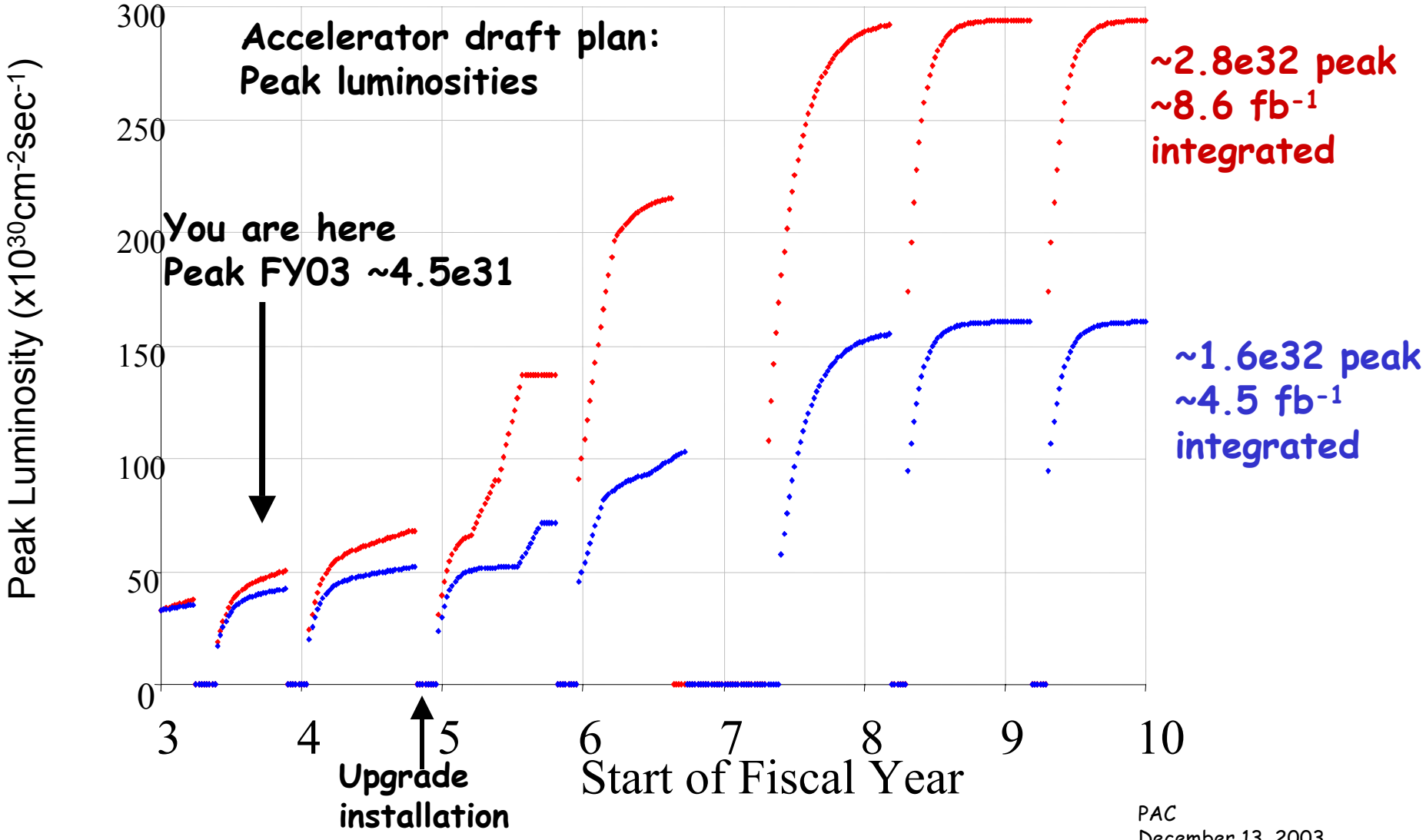
Run IIb Upgrade Project

- Project Status Overview
- Technical progress
  - Silicon Layer 0 detector
  - Trigger/DAQ
- Installation/Commissioning plans
- Cost & Schedule
- Summary

Run 2B upgrade

- Project recently rebaselined
  - Full silicon detector upgrade cancelled
    - Descoped version with only inner layer of silicon approved
      - While not as powerful as the full 6 layer upgrade, it will mitigate risk of losing significant tracking ability as current detector ages
  - Trigger upgrade continued
    - Additional readout electronics conditionally approved
      - New electronics for central fiber tracker
      - Helps tracking efficiency in higher luminosity/occupancy environment
  - DAQ/Online systems upgrade continued
    - Upgrade level 3 processing power, database & host servers, control systems

Run IIb Luminosity Projections



Run 2B upgrade

- Maintain tracking and b-tagging efficiency
  - higher luminosity environment
  - Mitigate risk for ageing silicon detector
    - Full Run IIb silicon upgrade cancelled => addition of inner layer silicon detector (layer 0)
- Maintain data taking efficiency in high rate environment
  - Trigger upgrade
    - Improve L1 Cal jet finding efficiency
    - Allow triggering on tracks matched to calorimeter energy
    - Improved L1 track finding efficiency
    - Level 2 processor upgrades for more complex algorithms
    - Silicon Track Trigger expansion to accommodate Layer 0
    - New readout electronics for central fiber tracker
  - DAQ/Online systems
    - Upgrade level 3 processing power, database & host servers, control systems

Run IIb Project Organization
Nov '03

Full Run IIb silicon replacement, now cancelled, was WBS 1.1

DØ Run IIb Project
J. Kotcher, Project Manager
V. O'Dell, Deputy (Trigger/DAQ); R. Lipton, Deputy (Silicon Layer 0)
W. Freeman, Associate; M. Johnson, Technical Coordinator
D. Knapp, Budget Officer; T. Erickson, Administration

WBS 1.2 Trigger
P. Padley
D. Wood

- 1.2.1 L1 Cal Upgrade — M. Abolins, H. Evans
- 1.2.2 L1 Cal/Track Match — K. Johns
- 1.2.3 L1 Track Trigger — M. Narain
- 1.2.4 L2β Upgrade — R. Hirosky
- 1.2.5 Silicon Track Trigger — U. Heintz
- 1.2.6 Simulation — E. Barberis, M. Hildreth
- 1.2.7 Administration — (D. Wood)
- 1.2.8 AFE II/TriP — A. Bross

WBS 1.3 DAQ/Online
S. Fuess

- 1.3.1 Level 3 Systems — D. Chapin, G. Watts
- 1.3.2 Network & Host Systems — J. Fitzmaurice, S. Krzywdzinski
- 1.3.3 Control Systems — F. Bartlett, G. Savage, V. Sirotenko
- 1.3.4 DAQ/Online Management — (S. Fuess)

WBS 1.4 Project Administration

WBS 1.5 Installation
R. Smith

- 1.5.1 Silicon Installation — Mechanical: (W. Cooper) Electronics: (L. Bagby)
- 1.5.2 Trigger Installation — D. Edmunds

WBS 1.6 Silicon Layer 0
A. Bean
(R. Lipton)

- 1.6.1 Sensors — M. Demarteau, R. McCarthy
- 1.6.2 Readout Elec — A. Nomerotski, R. Sidwell
- 1.6.3 Mech Des & Fabrication — W. Cooper
- 1.6.4, 1.6.5 Detector Modules & Integ — L. Bagby, J. Fast
- 1.6.6 Administration — (A. Bean)

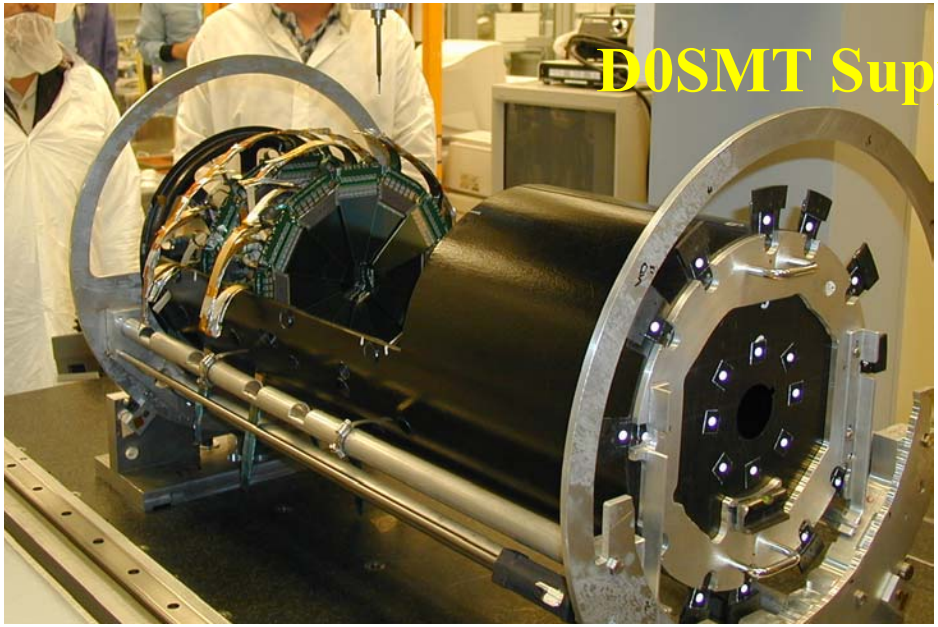
Installation an integrated part of project plan, but removed from formal Run IIb baselining

Layer 0 Silicon Detector

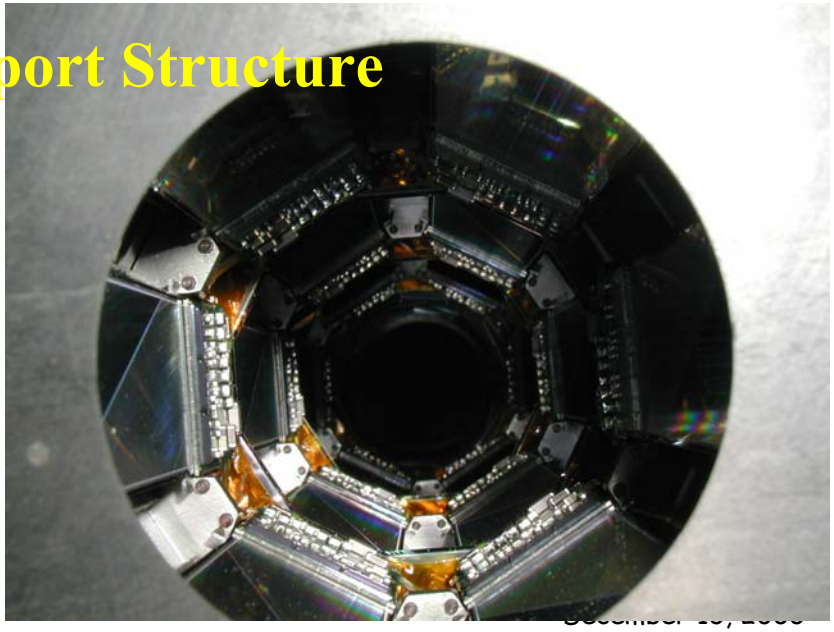
Layer 0 Project

DZERO Layer 0 is a silicon detector *inside* the current inner layer. This detector will

- Mitigate tracking losses due to radiation damage and detector failure
- Provide more robust tracking and pattern recognition for higher luminosities
- Improve impact parameter resolution



D0SMT Support Structure



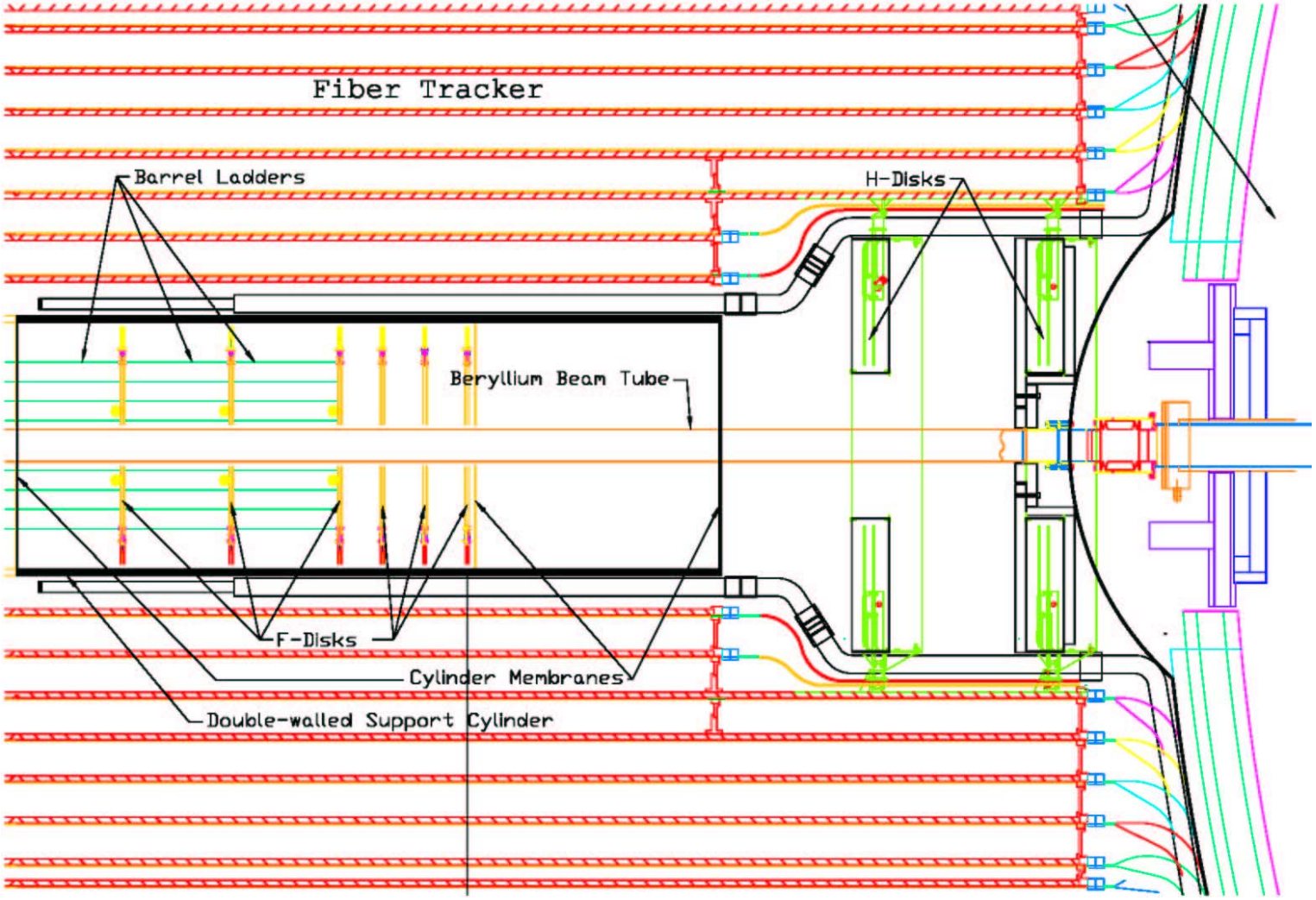
Silicon Layer 0 Institutions

Layer 0 institutions

- Brown, California State University Fresno, CINVESTAV Mexico, Fermilab, University of Illinois Chicago, Kansas State University, Kansas University, Louisiana Tech University, Michigan State University, Moscow State University, Northwestern University, Rice University, University of Rochester, SUNY-SB, University of Washington

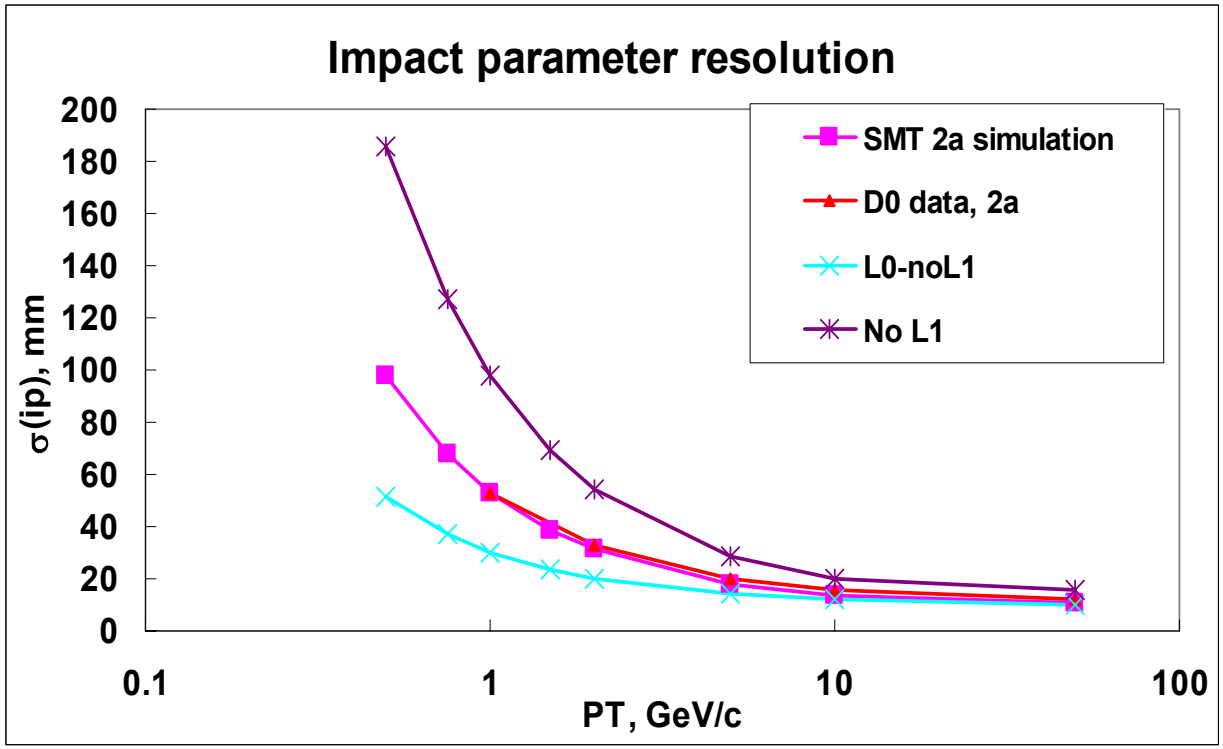
- Lots of university involvement
- Large MRI grant (~$650k)
- Additional in-kind university support

Layer 0 Project



Layer 0 Simulations

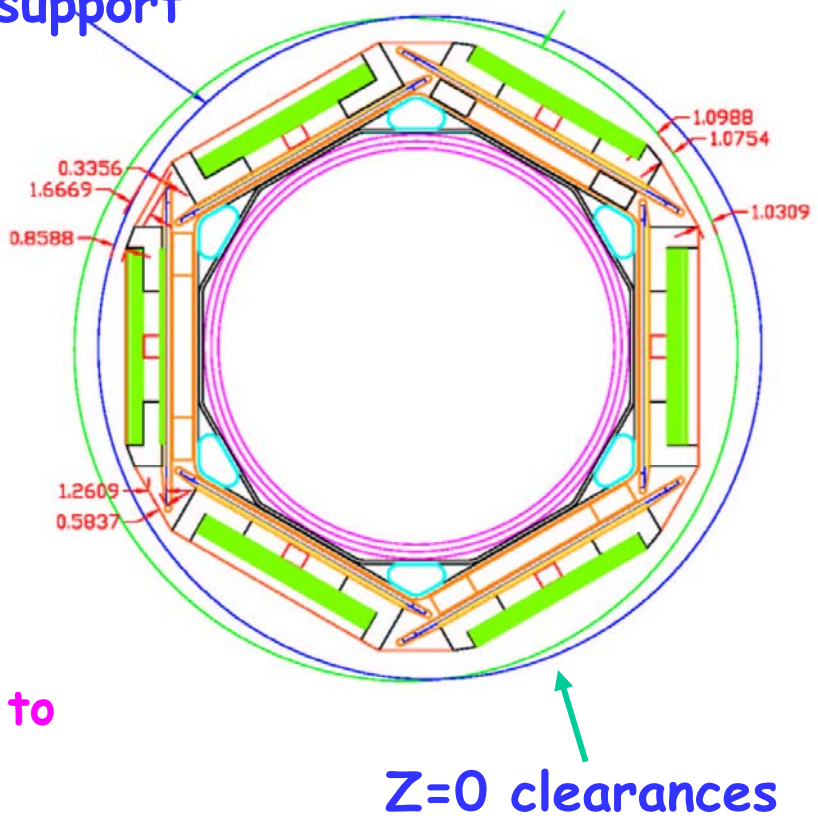
- We expect layer 1 Micron sensors to begin to fail at exposures of ~ 3-4 fb^{-1} (+- 50%)
- We are seeing continuing failures of readouts in the current detector (~90% currently good)



- Improvement in impact parameter resolution,especially at low momentum
- Translates directly into enhanced b tagging efficiency

Layer 0 Design

- Design – use as much of the Run2b R&D as possible
- Detector must fit in 22.8 mm SMT support structure opening
  - Six phi segments – match STT
  - Eight z segments 2x7,2x12cm
  - Analog cables – low mass
  - 48 HDIs x 256 channels
  - SVX4 chips (96)
- Replace at least outer H disks
- Sensor pitch – 71 μm (inner), 81 μm (outer)
  - Increases phi acceptance to 98.4%
  - Equal (71μm) pitch limits acceptance to 93.1%
  - Can be read out with one cable type

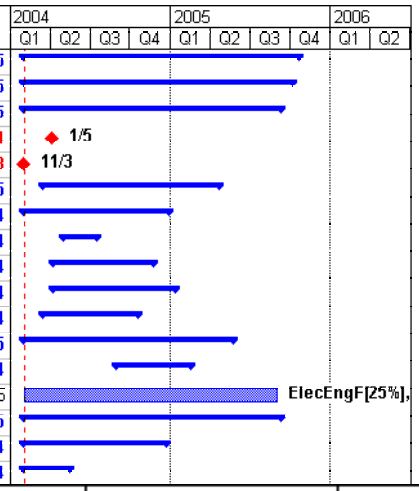


Comparison with Run2b Inner Layer

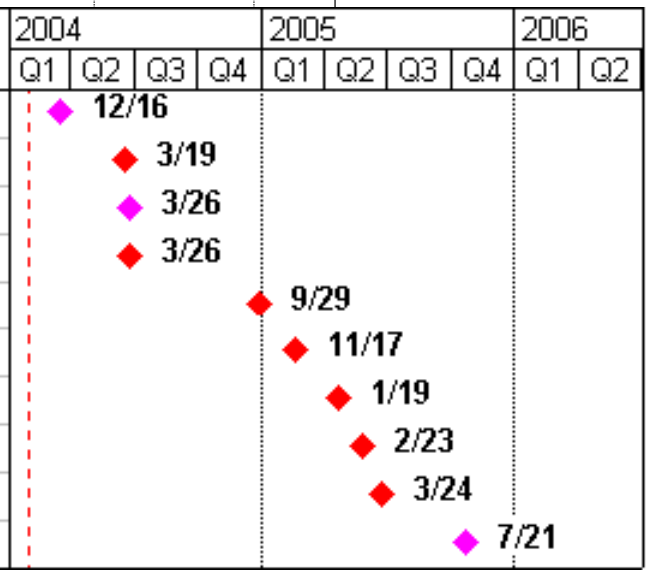
	Silicon Layer 0	Run2b Inner Layer
Sensors # Pitch(int, readout) Length	6 ϕ x 8 z = 48 (35/71),(40/81) 7, 12 cm	12 ϕ x 12 z = 144 (25/50) μm 7.7 cm
Analog Cables	4 lengths, <36 cm Double sensor pitch	6 lengths, <43.5 cm Double sensor pitch
Support	Six-sided nested structure (simpler)	Twelve-sided crenelated structure
Hybrids	Identical, use SVX4	
Junction cards, twisted pair and Digital cables	Identical design	
Adapter cards	Redesign to allow isolation of layer 0	

New Fully Resource Loaded Schedule

ID	WBS	Task Name	Duration	Start	Finish
1	1.6	Layer 0 Silicon Detector	424 d	Mon 11/3/03	Thu 7/21/05
2	1.6.1	Sensors	415 d	Mon 11/3/03	Fri 7/8/05
16	1.6.2	Readout Electronics	395 d	Mon 11/3/03	Thu 6/9/05
17	1.6.2.1	SVX4 Chips Available	0 w	Mon 1/5/04	Mon 1/5/04
18	1.6.2.2	SASEQ Test Stands Available	0 w	Mon 11/3/03	Mon 11/3/03
19	1.6.2.3	Hybrids	265 d	Wed 12/17/03	Wed 1/19/05
40	1.6.2.4	Analog Cables	225 d	Mon 11/3/03	Wed 9/29/04
49	1.6.2.5	Flex Grounding Circuits	55 d	Mon 2/2/04	Fri 4/16/04
54	1.6.2.6	Digital Cables	160 d	Fri 1/9/04	Tue 8/24/04
64	1.6.2.7	Twisted-Pair Cables	195 d	Fri 1/9/04	Wed 10/13/04
74	1.6.2.8	Junction Cards	145 d	Wed 12/17/03	Tue 7/20/04
82	1.6.2.9	Adapter Cards	320 d	Mon 11/3/03	Wed 2/23/05
95	1.6.2.10	High-Voltage System	120 d	Tue 6/1/04	Wed 11/17/04
100	1.6.2.11	Readout Chain Integration	78 w	Mon 11/3/03	Thu 6/2/05
101	1.6.2.12	Full Chain Tests	395 d	Mon 11/3/03	Thu 6/9/05
108	1.6.3	Mechanical Design and Fabrication	220 d	Mon 11/3/03	Wed 9/22/04
109	1.6.3.1	Support Structures Design	65 d	Mon 11/3/03	Fri 2/13/04
117	1.6.3.2				
118	1.6.3.3				
122	1.6.3.4				
126	1.6.3.5				
130	1.6.3.6				
131	1.6.3.7				
139	1.6.3.8				
140	1.6.4				
169	1.6.5				
195	1.6.6				



ID	Milestone
112	Freeze Mechanical Parameters
9	Release Sensors for Production
24	Release Hybrids for Production
45	Release Analog Cables for Production
48	All Analog Cables Delivered and Tested
15	All Sensors Delivered and Tested
39	All L0 Hybrids Delivered, Stuffed, and Tested
94	All Adapter Cards Delivered and Tested
163	Silicon L0 Module Production Complete
191	Layer 0 Silicon Detector Ready to Move to DAB



Higher level milestones (subset of full milestone list)

Silicon Layer 0 costs

- Unburdened FY02 $

	FY 02 $ no G&A	M&S non-labor	M&S Labor	M&S Cost	Contingency %	M&S Contingency	Total M&S	FNAL Labor	Labor Contingency %	Labor Contingency	Total Labor	Total Cost (incl labor	Cost + Contingency
1	Layer 0 Silicon Detector	$573,805	$208,379	$782,184	73%	$573,426	$1,355,610	$535,847	50%	$267,923	$803,770	$1,374,921	$2,216,270
1.1	Sensors	$163,000	$1,200	$164,200	100%	$164,200	$328,400	$14,940	50%	$7,470	$22,410	$179,140	$350,810
1.2	Readout Electronics	$281,708	$117,840	$399,548	76%	$303,461	$703,009	$198,629	50%	$99,314	$297,943	$619,577	$1,022,352
1.3	Mechanical Design and F	$49,686	$89,339	$139,025	50%	$69,413	$208,438	$134,192	50%	$67,096	$201,288	$273,217	$409,726
1.4	Layer 0 Detector Modules	$16,711	$0	$16,711	75%	$12,503	$29,214	$74,076	50%	$37,038	$111,114	$90,787	$140,328
1.5	Final Detector Integration	$25,700	$0	$25,700	50%	$12,850	$38,550	$60,202	50%	$30,101	$90,303	$85,902	$128,853
1.6	Monitoring	$12,000	$0	$12,000	50%	$6,000	$18,000	$0		$0	$0	$12,000	$18,000
1.7	Software and Simulation	$0	$0	$0		$0	$0	$42,300	50%	$21,150	$63,450	$42,300	$63,450
1.8	Silicon Project Administra	$25,000	$0	$25,000	20%	$5,000	$30,000	$11,508	50%	$5,754	$17,262	$71,998	$82,752

- Note that a large part of the M&S costs (~$690k) are covered through the existing MRI grants for the Run IIb Silicon Upgrade
- Fully burdened cost of Layer 0 is $1.6M plus 55% contingency

Layer 0 progress

- Definition of all basic parameters Dec 15
  - Start of sensor, analog cable design and procurement
- No prototype phase for most components
  - Quantities small prototype = production
  - Run2b prototypes already complete for many items
  - Includes prototyping for adapter cards, supports
- Hybrids critical path – received new shipment last month – may be usable unchanged
- Six month sensor production – based on Run2b experience but will be critical path if ~2 months late. Sensor order date – March 19.
  - First contact with Hamamatsu extremely positive
- ~1.5 year design/construction – Finish 7/21/2005

Run 2b Trigger/DAQ Upgrade

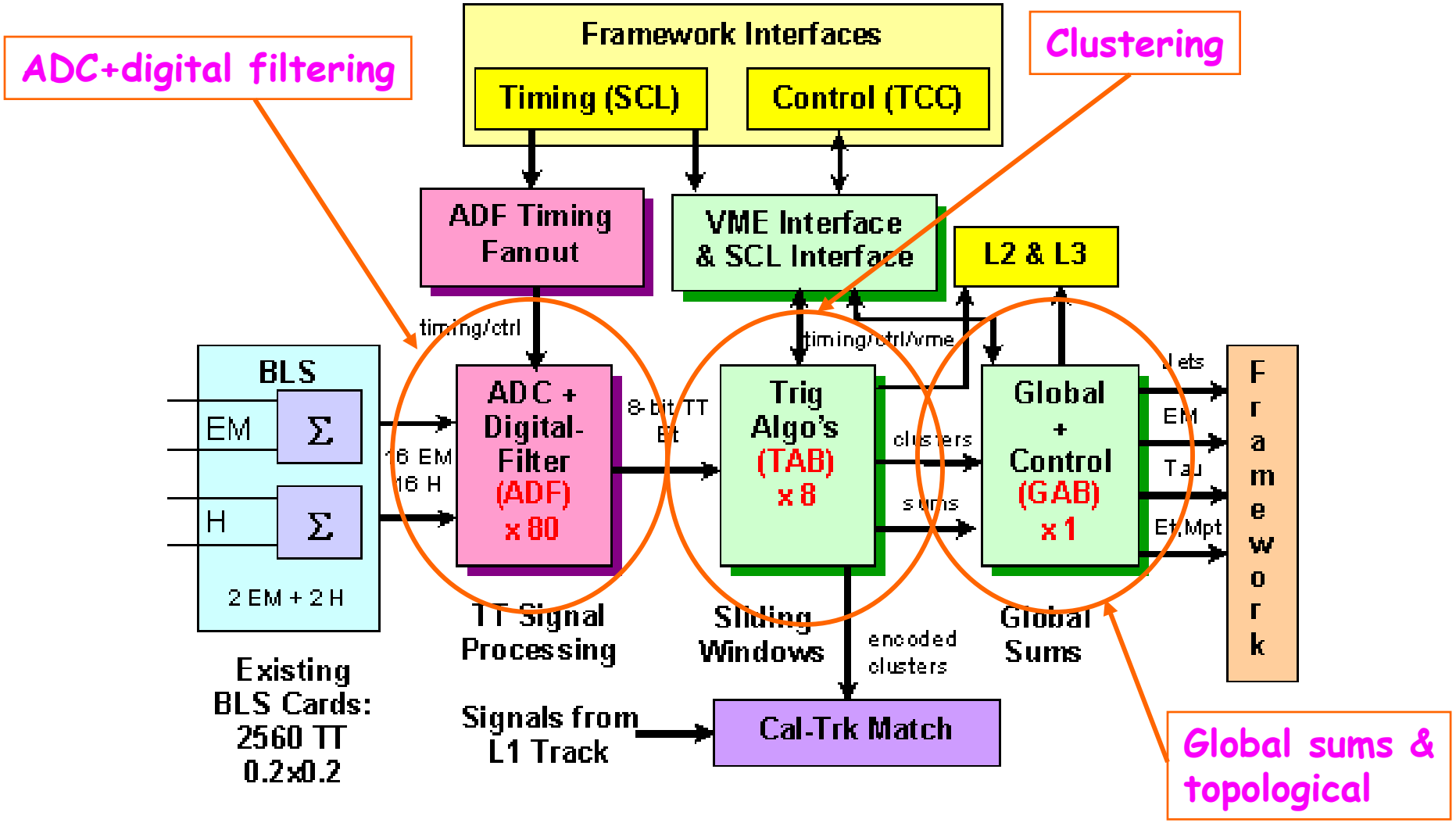
Ingredients of the Trigger Upgrade

- Level 1
  - Calorimeter trigger upgrade
    - sharpens turn-on trigger thresholds
    - more topological cuts
  - Calorimeter track-match
    - fake EM rejection
    - tau trigger
  - L1 tracking trigger upgrade (CTT)
    - improved tracking rejection especially at higher occupancies
- Level 2
  - L2 Processor upgrades for more complex algorithms
  - Silicon Track Trigger expansion
    - More processing power
    - use trigger inputs from new silicon layer 0
- New Readout Electronics for Central Fiber Tracker

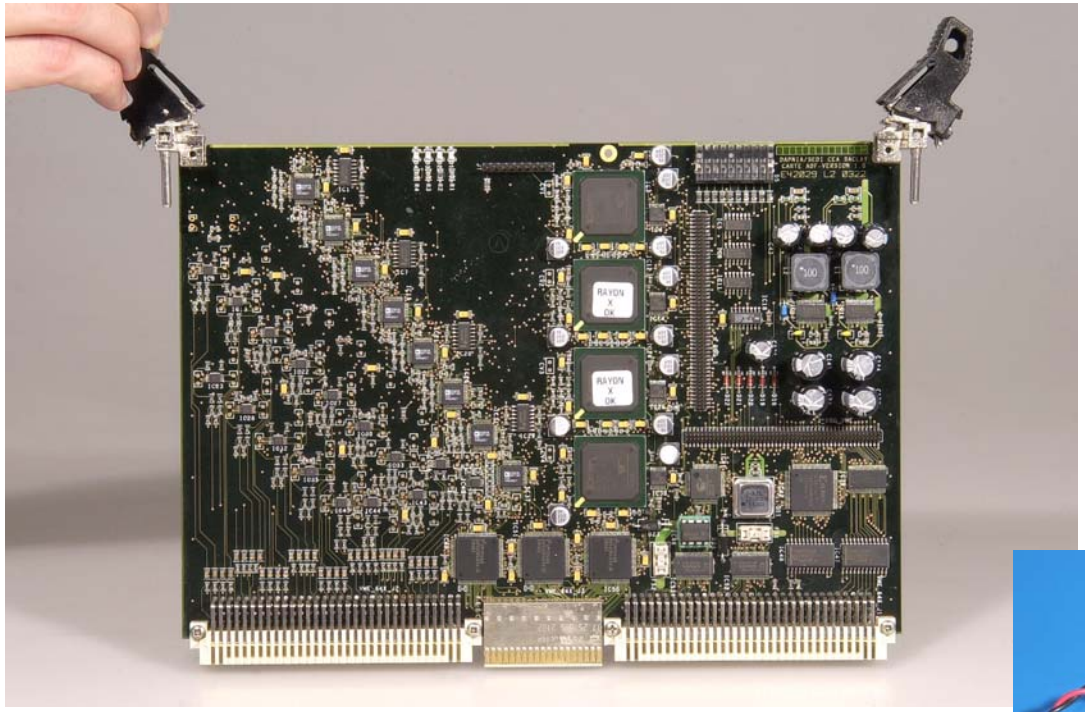
Trigger Upgrade Project Institutions

Sub-project	Institution(s)
Calorimeter: ADF	Saclay, MSU, UIC, Virginia
Calorimeter: TAB	Columbia
Track trigger	Boston U., FNAL
Cal-Track match	U. of Arizona
Simulation & algorithms	Notre Dame, Saclay, Kansas, Manchester, Brown
Online software & integration	MSU, Northeastern, FSU,Langston
Level 2β	Orsay, Virginia, MSU
STT upgrade	Boston, Columbia, Stony Brook, FSU

Upgrade L1 Cal Trigger

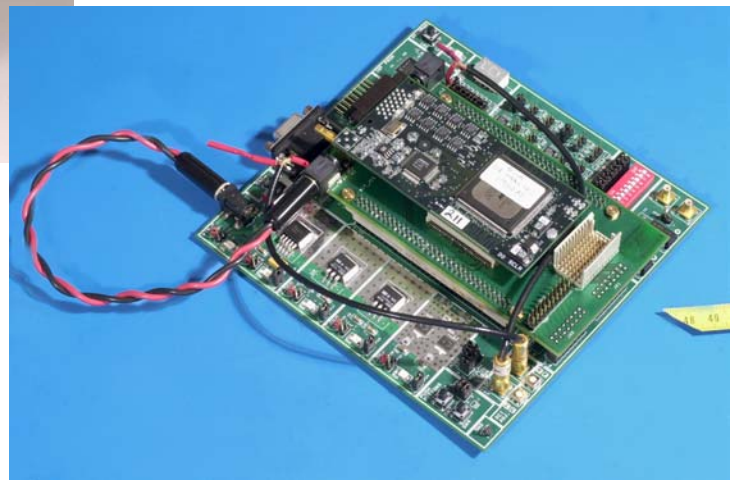


ADF Prototype



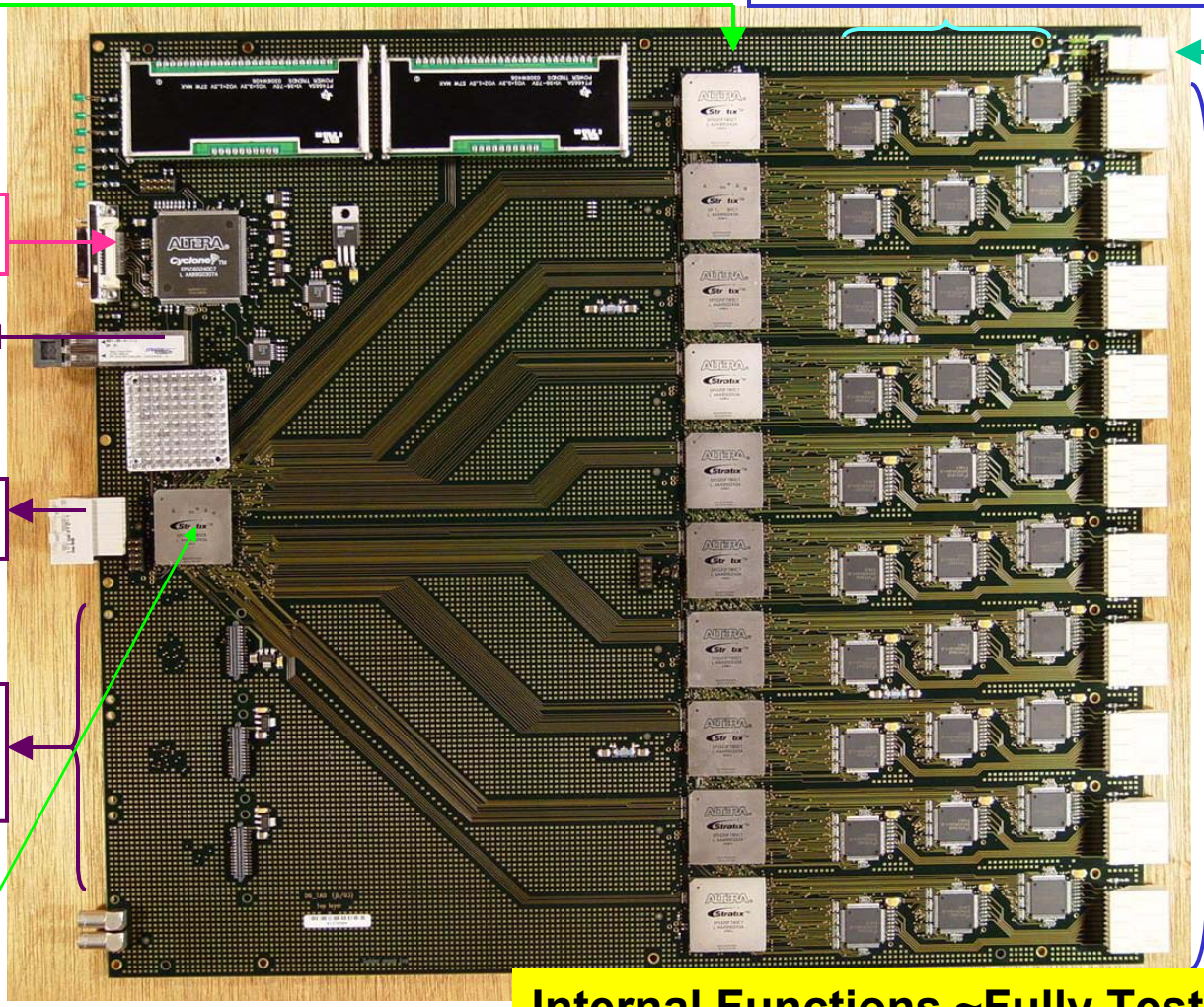
ADF Prototype board

Underwent integration tests at Fermilab, Oct 03



Prototype ADF Timing Card

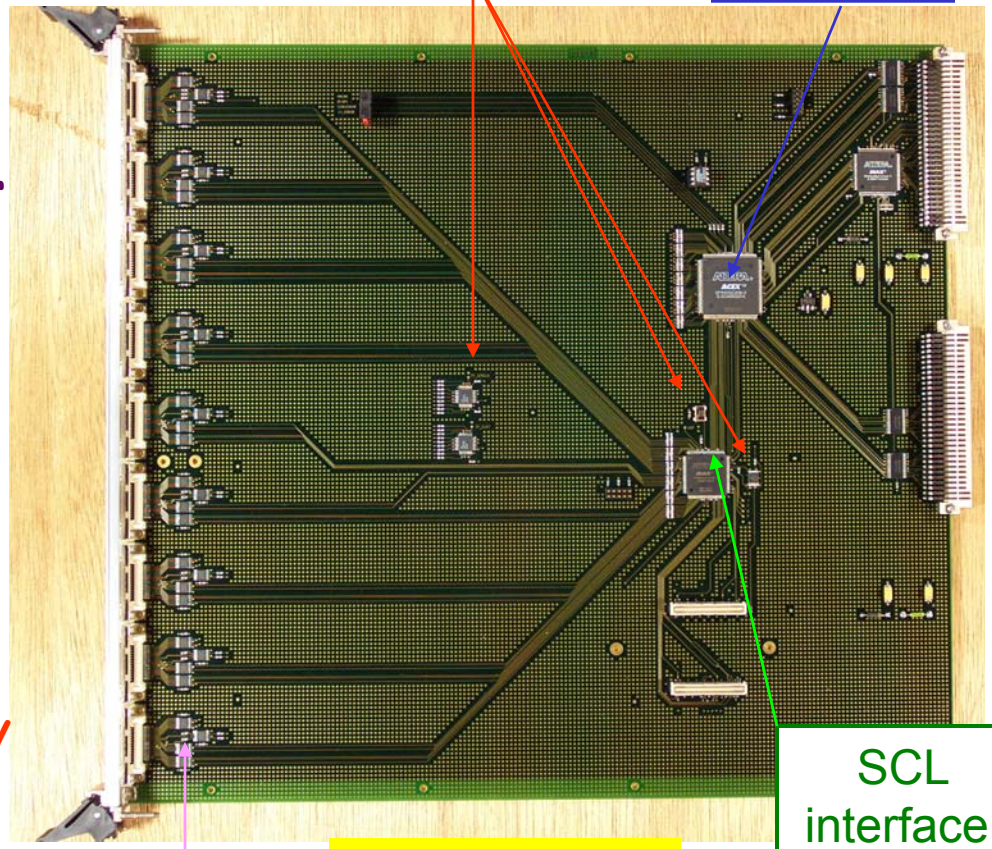
TAB Prototype



Internal Functions ~Fully Tested

VME/SCL Board

- New Comp. of TAB/GAB system
  - proposed: Feb 03
  - change control: Mar 03
- Interfaces to
  - VME (custom protocol)
    - not enough space on TAB for standard VME
  - D0 Trigger Timing (SCL)
  - (previously part of GAB)
- Why Split off from GAB
  - simplifies system design & maintenance
  - allows speedy testing of prototype TAB
- Prototype at Nevis: May 12
  - main VME & SCL functionality tested & working



TAB/GAB Test Card

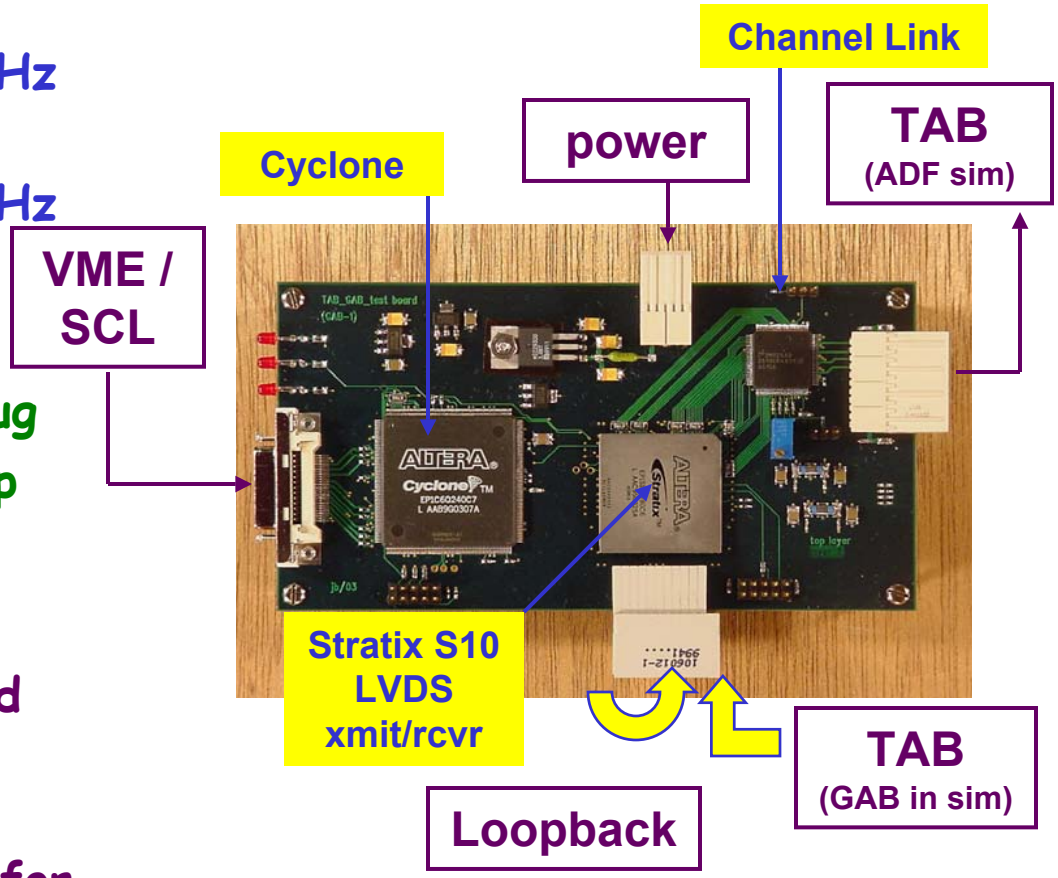
TAB/GAB Data Rates

- TAB: LVDS 424 MHz
  - (channel link)
- GAB: LVDS 636 MHz
  - (stratix)

Test Card at Nevis

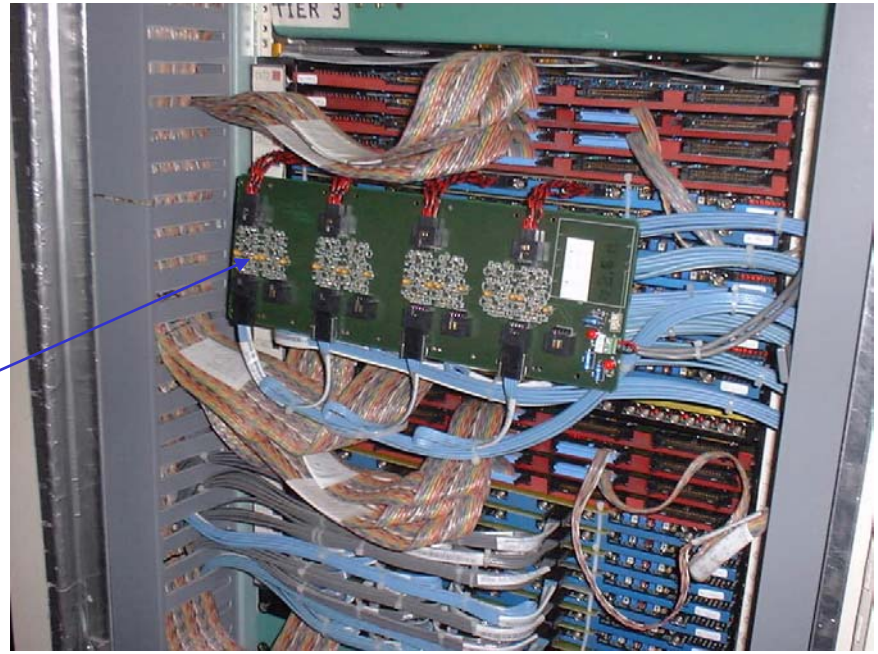
- Start Design mid-Aug
- Board at Nevis 29-Sep
- Cost ~$2K

- Status
  - ADF-to-TAB xmit tested before integration
  - Will test TAB-to-GAB before sending out GAB for fabrication



Signal Splitter

- Access to Real Trigger Tower Data using "Splitter" Boards
  - designed/built by Saclay
  - active split of analog signals at CTFE input
  - 4 Trigger Towers per board
  - installed: Jan. 2003



- Splitter Data
  - no perturbation of Run IIa L1Cal signals
  - allows tests of digital filter algorithm with real data

Prototype Integration Tests

- First test of Serial Command Link (SCL) → TAB done in 9-17 October
- Tests with ADF + TAB prototypes
  - SCL → VME/SCL → TAB, ADF
  - BLS Data (split) → ADF → TAB
  - Flexible, staged schedule allows components to be included as they become available
- Set up semi-permanent Test Area outside of Movable Counting House
  - connection to SCL, split data signals
  - allows L1Cal tests without disturbing Run IIa data taking

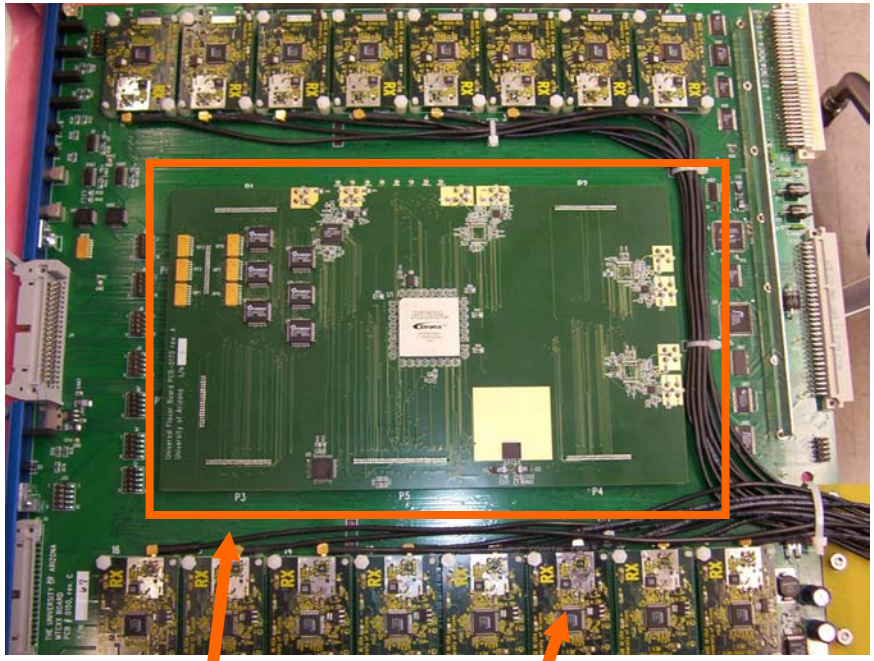
Successful integration tests this fall

ADF->TAB

TAB -> L1mu (L1cal-track surrogate)

L1 Cal Track Match

- UFB (Flavor Board)
  - Prototypes in hand
  - Boundary scan and downloading OK
  - Receiver/transmitter testing in progress
  - L1MU "05" algorithm implemented in Stratix EP1S20F780C7
    - (simulated but not tested)
  - $H \rightarrow \tau\tau$ algorithm implementation in progress

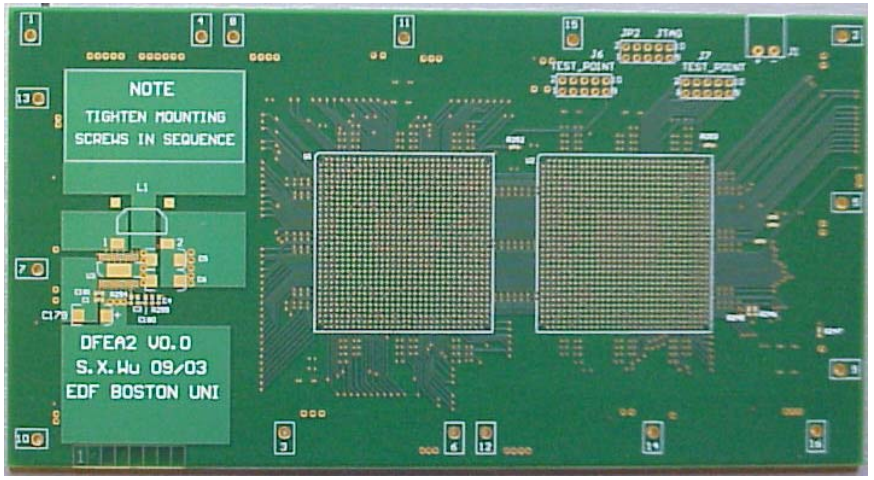


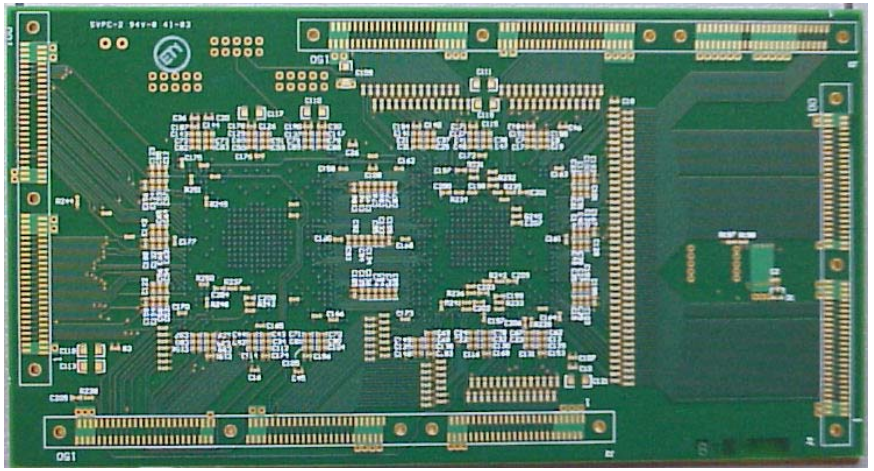
MTCxx (mother)
Run IIa version

Universal Flavor board (daughter)
Run IIb prototype

L1 Central Track Trigger

- Digital Front End Axial (DFEA) daughter cards get replaced with new layout with larger FPGA's (Xilinx Virtex-II XC2V6000)
  - Allows more complicated equations for using narrower roads to lower trigger rate at higher occupancies
  - Only 80 daughter cards get replaced;
  - rest of Run IIa system remains intact
- Implemented prototype firmware (Boston U)
  - Includes equation files from all 4 momentum bins
  - DFEA logic is implemented in two FPGAs





Central Fiber Tracker readout upgrade (AFE II)

- AFE II + TriPT will
  - Improve noise floor and pedestal stability which will allow for consistent and reliable threshold setting at the level of 1.5 pe
    - Better hit efficiency and point resolution
  - Readout architecture much more flexible
    - Less deadtime
    - With additional memory, buffers can be added to greatly increase L1 capability
  - Added functionality of the Trip*t* (z information)
    - Large reduction in track reconstruction time
  - Elimination of SIFT, SVXIIe, and MCM in readout should greatly reduce board maintenance load

- R&D for AFE is going well
  - Expect prototype AFE + TRiP late spring/early summer
  - This part of the project is only conditionally approved
    - Plan to test prototype, compare with simulations
    - Hold D0 internal review
    - Hold laboratory review
  - If all reviews successful, then will go ahead with project

DAQ/Online

System	Items	Need
Level 3 filter nodes	96 more L3 Farm nodes	Match to rates and processing requirements
DAQ HOST system	Linux data logging nodes and buffer disk arrays	Replace existing systems with higher performance nodes
ORACLE systems	Database nodes, disk arrays, and backup systems	Adopt lab standard ORACLE platform
File Server systems	Linux server nodes, disk arrays, and backup systems	Provide increased storage capacity
Slow Control system	VME processors for control and monitoring of detector	Improve monitoring performance for extended run

Upgrades to DAQ/Online systems required for long-term, high rate running during Run IIb

Installation/Commissioning

Upgrade installation and commissioning

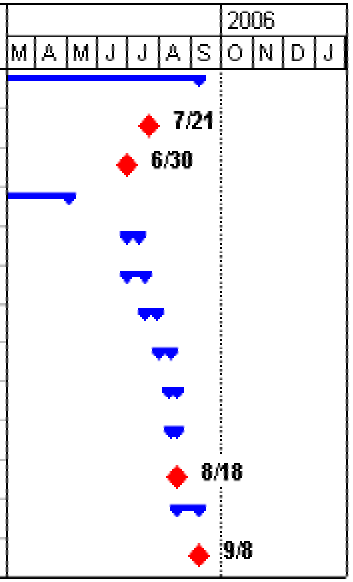
Installation/Commissioning

- Plan to install/commission during planned accelerator shutdowns as much as possible
  - want to install as early as possible to get the most benefit
  - want to install during machine shutdowns
- 2 phases of commissioning
  - technical commissioning
    - testing inputs/outputs and integration
    - no beam necessary
  - physics commissioning
    - need beam for this
    - trigger verification/calibration

L0 Installation/Commissioning

- Installation not part of formal project but:
  - Fully resource loaded project plan

ID	WBS	Task Name	Duration	Start	Finish
2	1.5.1	Layer 0 Silicon Installation	84.4 w	Mon 1/5/04	Thu 9/8/05
3	1.5.1.1	Silicon Ready To Move To DAB	0 w	Thu 7/21/05	Thu 7/21/05
4	1.5.1.2	Shutdown for Installation Begins	0 w	Thu 6/30/05	Thu 6/30/05
5	1.5.1.3	Prepare Silicon Infrastructure	66.6 w	Mon 1/5/04	Tue 5/3/05
17	1.5.1.4	Open Detector and Install CC-EC Scaffolding	1.2 w	Thu 6/30/05	Mon 7/11/05
26	1.5.1.5	Remove RunIIa Beampipe, H Disks	2.2 w	Thu 6/30/05	Mon 7/18/05
32	1.5.1.6	Install RunIIb L0 Silicon Detector	2 w	Mon 7/18/05	Fri 7/29/05
38	1.5.1.7	Cable L0 Silicon, Reconnect Cooling System	1.8 w	Mon 8/1/05	Thu 8/11/05
44	1.5.1.8	Reconnect Tev Beam Tube	1.2 w	Thu 8/11/05	Thu 8/18/05
48	1.5.1.9	Technical commissioning of detector	1 w	Fri 8/12/05	Thu 8/18/05
50	1.5.1.10	Silicon Ready for Resumption of Tevatron Operation	0 w	Thu 8/18/05	Thu 8/18/05
51	1.5.1.11	Commission Online Readout Software, Close Detector	2.8 w	Fri 8/19/05	Thu 9/8/05
54	1.5.1.12	Silicon System Ready for Physics Commissioning	0 w	Thu 9/8/05	Thu 9/8/05



- Rolled up task list
- Shutdown time for installation: 6 weeks (Tevatron off)
- Ready for physics commissioning: 9 weeks

Upgrade Installation/Commissioning

- Resource loaded installation/technical installation plan for full upgrade (L0, Trigger)
- L0 installation requires long access to collision hall
- Other upgrade pieces do not require access (or very short access)
  - Most done "adiabatically" (CTT, L2β, etc.)
  - AFE installation under study but unlikely to require extended access
  - Largest perturbation to experiment: L1 Calorimeter trigger (have to decommission existing trigger).
    - Plan to shadow L0 Tevatron shutdown
- Collaboration wide task force being formed to examine detailed impact of commissioning for each upgrade part
  - Formal internal review process to determine installation readiness

Upgrade Trigger Installation/Commissioning Plans

- L1 Cal trigger: Summer '05
  - L1 Cal trigger pre-tested on sidewalk
  - we can then install + technically commission L1 cal in 10 weeks (6 + 4)
  - useful L1 Cal trigger ~ 2 weeks after resumption of Tevatron
    - use 2 weeks with beam to verify trigger
  - fully calibrated will take longer, depending on reliability/luminosity of TeV (~1 month)
    - Precision calibration in parallel with data taking
- L1cal-track
  - System commissioned with L1mu modules, then replaced with real L1cal-track modules
  - Ready in advance for L1cal inputs
- L2 STT
    - installed/technically commissioned during Layer 0 installation
- adiabatic installation of CTT (starting early '05)
  - replace modules while still running in run2a mode
- L2β can be upgraded earlier - whenever necessary

Cost/Schedule Summary

Total MIE Rebaseline Costs

Project Total Equipment Cost (DOE MIE)

DOE TEC, by subsystem in AYk$	Total	Cont. only	EQ base	G&A only
Silicon	1824	893	735	196
Trigger	5595	1676	3268	651
DAQ/Online	1389	327	881	181
Project Administration	1151	227	729	195
TOTAL	9959	3124	5613	1222

Contingency fraction on MIE portion = 45%

- Total DOE cost (fully burdened, AY$)
- Does not include MRI (Trigger, Silicon L0) or University inkind

Director's Milestones

D0 Detector Upgrade
Director's Milestones
Forecast Dates

Fiscal Year

Task Name	Forecast Date
1.6 Layer 0 Silicon	
Freeze Mechanical Parameters	12/16
Release Sensors for Production	3/19
Release Hybrids for Production	3/26
Release Analog Cables for Production	3/26
All Analog Cables Delivered and Tested	9/29
All Sensors Delivered and Tested	11/17
All L0 Hybrids Delivered, Stuffed, and Tested	1/19
All Adapter Cards Delivered and Tested	2/23
Silicon L0 Module Production Complete	3/24
Layer 0 Silicon Detector Ready to Move to DAB	7/21
1.2 Trigger	
L1 Calorimeter Trigger TAB/GAB Prototyping Complete	3/1
Start Production TAB Fabrication	10/25
L1 Trigger Cal-Trk Match Production and Testing Completed	10/29
L2 Silicon Track Trigger Production and Testing Complete	1/31
L1 Central Track Trigger Production And Testing Complete	2/23
L2 Beta Trigger Production And Testing Complete	2/28
L2 Trigger Upgrade Production and Testing Complete	2/28
L1 Calorimeter Trigger Production And Testing Complete	7/5
L1 Trigger Upgrade Production and Testing Complete	7/5
1.3 Online	
Online System Production and Testing Complete	6/17

planning to finish 07/05 for a summer/fall 2005 installation

PAC
December 13, 2003

Conclusions

- Project presented here represents full scope for rebaselined Run IIb DZero Detector Project
  - Has gone through laboratory change control and review
  - Full baseline change proposal + supporting documentation was submitted Nov 30
  - ESAAB December 8 for rebaselining + CD3b
    - Approved
- Project is making impressive technical progress despite these distractions
  - Trigger solidly in prototype testing phase
    - Major L1 Cal integration milestones met this fall
  - Layer 0 springboarding off of Run IIb R&D and moving quickly
- Installation/Commissioning plans firming up
  - Planning to install during 2005 summer/fall shutdown